IN THE CLAIMS

Claims 1-20 (Canceled)

21. (previously presented) A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming an inter-layer insulating layer on a substrate;

forming a storage node contact connected to the substrate by passing through the inter-layer insulating layer;

forming a storage node supporting layer on the inter-layer insulating layer in a manner that an insulating layer is inserted into a space between a first etch barrier layer and a second etch barrier layer;

forming a storage node oxide layer on the second etch barrier layer;

forming a storage node hole exposing the storage node contact by etching the first and the second etch barrier layers, the insulating layer, and the storage node oxide layer; and

forming a cylindrical storage node electrically connected to the storage node contact.

22. (Canceled)

23. (previously presented) The method as recited in claim 33, wherein the step of selectively removing the storage oxide layer and the insulating layer is proceeded by employing a wet type dip-out process.

24. (previously presented) The method as recited in claim 33, wherein the insulating layer is an oxide layer formed through a chemical vapor deposition technique, and the first and the second etch barrier layers are nitride layers.

25. (Original) A method for fabricating a capacitor of a semiconductor device, comprising the steps of:

forming an inter-layer insulating layer on a substrate;

forming a storage node contact connected to the substrate by passing through the inter-layer insulating layer;

forming a storage node supporting layer on the inter-layer insulating layer in a manner that an insulation layer is inserted into a space between a first etch barrier layer and a second etch barrier layer;

forming a storage node insulating layer on the storage node supporting layer;

forming a storage node hole by etching the storage node insulating layer and the storage node supporting layer to make an etching process be stopped at the first etch barrier layer;

removing selectively the storage node insulating layer and the storage node supporting layer to widen a width of the storage node hole and simultaneously form an under-cut region in between the second etch barrier layer and the first etch barrier layer;

forming a cylindrical storage node connected to the storage node contact as a bottom region of the storage node formed in the storage node hole is inserted into the under-cut region; and

removing selectively the storage node insulating layer.

26. (Original) The method as recited in claim 25, wherein, at the step of widening the width of the storage node hole and forming the under-cut region in between the second etch barrier layer and the first etch barrier layer, the storage node insulating layer and the storage node supporting layer are selectively etched through a dip process using a wet chemical.

27. (Original) The method as recited in claim 26, wherein the storage node insulating layer and the storage node supporting layer are oxide layers, and the first and the second etch barrier layers are nitride layers.

28. (Original) The method as recited in claim 26, wherein the dip process uses diluted HF, a chemical mixed with HF-based family or a chemical mixed with ammonia-based family and is proceeded at a temperature ranging from about 4 °C to about 180 °C for about 10 seconds to about 1800 seconds.

29. (Original) The method as recited in claim 25, wherein the step of removing selectively the storage node insulating layer is carried out at a temperature ranging from about 4 °C to about 180 °C for about 10 seconds to about 3600 seconds with use of a HF-based chemical.

30. (Original) The method as recited in claim 25, wherein the step of forming the storage node hole is carried out by employing a dry etching process.

31. (previously presented) The method as recited in claim 21, further comprising the step of removing selectively the storage node oxide layer.

32. (previously presented) The method as recited in claim 21, wherein the storage node oxide layer is formed with stacked layers having different etch selectivity values and determines a height of the storage node.

33. (previously presented) The method as recited in claim 32, wherein the step of forming the storage node hole includes further steps of:

forming a storage node mask on the storage node oxide layer;

etching the storage node oxide layer by using the storage node mask as an etching mask;

etching the second etch barrier layer and the insulating layer by using the first etch barrier layer as an etch barrier layer; and

removing selectively the storage node oxide layer and the insulating layer to thereby widen a width of the storage node hole and simultaneously form an under-cut region in between the second etch barrier layer and the first etch barrier layer.

34. (previously presented) The method as recited in claim 33, wherein the first and the second etch barrier layer have a thickness about 100 Å to about 2000 Å.

35. (previously presented) The method as recited in claim 34, wherein the insulating layer has a thickness of about 100 Å to about 3000 Å.

36. (previously presented) The method as recited in claim 35, wherein the storage node oxide layer uses one material selected from the group consisting of PETEOS, LPTEOS, PSG, BPSG, and SOG.

37. (previously presented) The method as recited in claim 23, wherein the dip process uses diluted HF, a chemical mixed with HF-based family or a chemical mixed with ammonia-based family and is proceeded at a temperature ranging from about 4 °C to about 180 °C for about 10 seconds to about 1800 seconds.

38. (previously presented) The method as recited in claim 37, wherein the step of removing selectively the storage node oxide layer is carried out at a temperature ranging from about 4 °C to about 180 °C for about 10 seconds to about 3600 seconds with use of a HF-based chemical.

39. (previously presented) The method as recited in claim 21, wherein the step of forming the storage node hole is carried out by employing a dry etching process.

40. (withdrawn) A capacitor for use in a semiconductor device, comprising:

a substrate;

an inter-layer insulating layer having a contact hole exposing a partial portion of the substrate and being formed on the substrate;

a storage node contact formed in the contact hole;

a storage node supporting layer formed in a manner that an insulating layer is inserted into a space between a first etch barrier layer and a second etch barrier layer and formed on the inter-layer insulating layer, wherein the storage node supporting layer includes a storage node hole exposing the storage node contact; and

a cylindrical storage node electrically connected to the storage node contact and supported by the storage node supporting layer.

41. (withdrawn) The capacitor as recited in claim 40, wherein the insulating layer is a nitride layer.

42. (withdrawn) The capacitor as recited in claim 40, wherein the first and the second etch barrier layer are an oxide layer.

43. (withdrawn) The capacitor as recited in claim 40, wherein the storage node contact is a polysilicon plug.

44. (withdrawn) The capacitor as recited in claim 42, wherein the first and the second etch barrier layer have a thickness about 100 Å to about 2000 Å.

45. (withdrawn) The capacitor as recited in claim 44, wherein the insulating layer has a thickness of about 100 Å to about 3000 Å.